UNIVERSIDADE NOVA DE LISBOA
FACULDADE DE CIÊNCIAS E TECNOLOGIA
DEPARTAMENTO DE ENGENHARIA ELECTROTÉCNICA

TAE

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Example of exam

Programa Doutoral - Tópicos Avançados em Electrónica (TAE)
(Advanced Topics in Electronics)

Exam 10/11 (5 pages)

1- CMOS technology

1.1 Currently, what is the most used integrated circuit technology in the world?

Select only one answer:

a) Bipolar technology ☐
b) BiCMOS technology ☐
c) GaAs technology ☐
d) CMOS technology ☐
e) None of the above ☐

1.2 Select the statement that is true from the ones below:

Select only one answer:

a) The power dissipation in digital CMOS circuits is inversely proportional to the square of the transistor channel length ☐
b) The gate leakage current in a CMOS technology with transistors with a smaller channel length is smaller than in a CMOS technology with transistors with a larger one. ☐
c) A MOS transistor with a smaller threshold voltage value has larger leakage current than a transistor with a larger threshold voltage value. ☐
d) The gate capacitance of a MOS transistor in the linear region is smaller than the gate capacitance of a MOS transistor in the saturation region. ☐
e) None of the above. ☐

1.3 Increasing the drain current in a MOS transistor results in:

Select only one answer:

a) a smaller V_{DSsat} voltage ☐
b) a larger DC gain of the device (gm/gds) ☐
c) a larger transition frequency (gm/Cgs) ☐
d) a smaller output noise ☐
e) None of the above. ☐

1.3 What noise source does not exist in a MOS transistor?

Select only one answer:

a) Thermal noise ☐
b) Flicker noise ☐
c) Shot noise ☐
d) All of the above ☐

2- Advanced Amplifier Topologies

2.1 In cascoded topologies of Operational Transconductance Amplifiers (OTAs), such as the folded-cascoded or the telescopic cascoded OTA, the expression for the GBW includes:

Select only one answer:

a) The *gm* of the cascode devices ☐
b) The *gm* of the common-source input devices used in the differential pair ☐
c) The *gds* of the cascode devices ☐
d) All of the above ☐
e) None of the above. ☐

2.2 In Miller-Compensated Two-stage OTAs, when we increase the value of the load capacitor (C_L) above a certain limit, the amplifier:

Select only one answer:

a) becomes more stable ☐
b) becomes unstable ☐
c) has a decrease in the DC gain ☐
d) has an increase in the DC gain ☐
e) None of the above. ☐

2.3 In a folded-cascoded OTAs if we double the DC biasing current in all devices (NMOS and PMOS):

Select only one answer:

a) The gain increases by 6 dB ☐
b) The gain increases by 3 dB ☐
c) The gain decreases by 6 dB ☐
d) The gain decreases by 3 dB ☐
e) None of the above ☐

2.4 In two-stage Miller-compensated OTAs, the ways to increase the GBW are:

Select only one answer:

a) increase the bias current of the devices used in the differential pair ☐
b) reduce the compensation capacitance, *Cc* ☐
c) reduce the V_{DSsat} of the devices used in the differential pair ☐
d) All of the above ☐
e) None of the above ☐

3- LNAs

3.1 Consider that the 1dB compression point at the output of a LNA is -20 dBm and its output dynamic range is 20 dB. Determine the minimum input signal power detectable by the LNA knowing that its power gain is 20 dB.

Select only one answer:

a) -40 dBm
b) -60 dBm
c) -80 dBm
d) -20 dBm
e) None of the above.

3.2 Figure 1 shows the input part of an integrated LNA in 130 nm technology for RF narrowband applications. The component L_s represents the inductance of the bonding wire which has approximately a 1 nH value. Calculate the value of transistor transition frequency ($f_T = g_m/C_{gs}$) needed to achieve a 50 Ω (real part) matching at the input ($Z_{in}=1/Y_{in}$) in resonance.

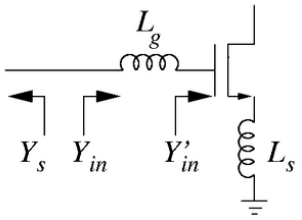

Figure 1 – LNA input.

(Suggestion: neglect the output transistor conductance g_{ds} and drain-gate capacitance C_{dg} in the simplified AC transistor model.)

Select only one answer:

a) $100x10^9$ Hz (100 GHz)
b) $5x10^9$ Hz (5 GHz)
c) $5x10^{10}$ Hz (50 GHz)
d) $20x10^9$ Hz (20 GHz)
e) None of the above.

3.3 In order to fully integrate a 600 MHz RF direct-conversion receiver in CMOS technology, the designer of the LNA and the following Mixer circuit should attend that:

Select only one answer:

a) is mandatory to include 50 Ω matching network between the two blocks.
b) is mandatory to include 75 Ω matching network between the two blocks.
c) the 50 Ω matching is not necessary since the distributed effects between the two blocks can be neglected and the signal is treated as a voltage one.
d) the 50 Ω matching is not necessary due to the low input impedance associated to the MOS transistor gate at low frequencies.
e) None of the above

4- Oscillators and Mixers

4.1- Accurate quadrature oscillators are required in low-IF receivers for:

Select only one answer:

a) Image rejection without external filtering. ☐
b) RF signal isolation. ☐
c) RF signal amplification. ☐
d) Converting the RF signal for the IF frequency. ☐
e) None of the above. ☐

4.2- The Barkhausen criteria is used in oscillator design:

Select only one answer:

a) Only in linear oscillators. ☐
b) Only in nonlinear oscillators. ☐
c) In all type of oscillators. ☐
d) Only in square signal oscillators. ☐
e) None of the above. ☐

4.3- The main advantage of the RC oscillator over the LC oscillator is:

Select only one answer:

a) Less phase noise. ☐
b) Lower power consumption. ☐
c) Occupies less chip area and do not need RF options. ☐
d) Less harmonic distortion ☐
e) None of the above ☐

4.4- The Gilbert Cell is a mixer of type:

Select only one answer:

a) passive. ☐
b) passive with parametric amplification. ☐
c) active single-balanced. ☐
d) active double balanced. ☐
e) None of the above. ☐

5 - CAD Tools

5.1 – In the presented optimization platform (ngEDA), the "chromosome" file includes:

Select only one answer:

a) The range values for the circuit variables, i.e., design space (e.g. width and length of transistors); ☐
b) The circuit indicators to be achieved; ☐
c) The fabrication technology parameters; ☐
d) All previous values; ☐
e) None; ☐

5.2 – The transistor's models used in the simulation/optimization phase allow:

Select only one answer:

a) Calculate the circuit performance; ☐
b) Compute the transient and dc I-V (current-voltage) characteristics; the parasitic elements (capacitances, resistances, inductances); ☐
c) All previous; ☐
d) None of the above; ☐

5.3- The design rules check (DRC) tools are to:

Select only one answer:

a) Verify the layout conformance against the foundry fabrication rules; ☐
b) Verify the layout conformance against the circuit netlist; ☐
c) Verify if the size of the elements (in layout) meet the circuit specifications ☐
d) None of the above; ☐

NAME:

Ph. D. Student #: